

In re: Won *et al.*
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In the Specification:

Please amend the Related Application section at page 1, lines 1-6 as follows:

Related Application

This application is a divisional of U.S. Application Serial No. 10/028,187, filed December 20, 2001, now United States Patent No. 6,653,186, which claims the benefit of priority from Korean Application No. 2000-82066, filed December 26, 2000, the disclosures of which are hereby incorporated herein by reference as if recited in their entirety.

Please replace the paragraph at page 7, lines 5-15, with the following amended paragraph:

As illustrated in FIG. 8, a first capacitor dielectric layer 112 is formed over the entire surface of the integrated circuit device. The first capacitor dielectric layer 112 is typically an amorphous layer that adheres well to the etch stop layer 108 and a subsequent U-shaped lower electrode, thus, the number of voids on the interface between the etch stop layer 108 and the first capacitor dielectric layer 112 may be reduced. The first capacitor dielectric layer 112 may include, for example, a dielectric material including tantalum oxide that may not be etched by an oxide etchant. The thickness of the first capacitor dielectric layer 112 is typically minimized to prevent an increase in capacitance. For example, if a second capacitor dielectric layer has a thickness of from about 100 to about 200 $[[D]]$ Å, the thickness of the first capacitor dielectric layer 112 is typically from about 10 to about 40 $[[D]]$ Å.

Please replace the paragraph at page 7, line 27 to page 8, line 2, with the following amended paragraph:

A conductive layer 114, *i.e.* a U-shaped lower electrode, is formed on the surface of the integrated circuit device as illustrated in FIG. 9. The conductive layer 114 is formed on the inner surface of the first capacitor dielectric layer 112, on the surface of the plug 104, and

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on the surface of the upper mold layer pattern 110. The conductive layer 114 may be formed using, for example, precious metal layers of a platinum group, such as a platinum (Pt) layer, a ruthenium (Ru) layer and an iridium (Ir) layer. The conductive layer 114 for the U-shaped lower electrode may have a thickness of from about 200 to about 500 [[D]] Å. The conductive layer 114 for the U-shaped lower electrode may be formed using a chemical vapor deposition (CVD) method having excellent step coverage.